Code No: D0605, D5509, D7701, D6801, D5701 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/AMY 2012
SYSTEM ON CHIP ARCHITECTURE
(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. a) Explain about MUO processors with a schematic. What are its salient features?
   b) What are the issues pertaining to design for low power consumption? Explain.

2. a) With the help of a schematic, explain about 3 and 5 stage pipeline ARM organization.
   b) How do you carryout ARM Co-processor interface? What are the issues involved? Explain.

3. How are ARM instructions classified? Explain about ARM processor instructions with suitable examples.

4. Explain about functions and procedures for ARM processor High Level Language with suitable examples.

5. a) Draw the circuit for Gate-Source Back biasing and explain its working, for the DRAM cell.
   b) Explain about Multi V_T and Dynamic V_T circuits.

6. a) Draw the circuit for on-chip voltage up-converter and explain the operation with the help of waveforms.
   b) Explain about various driving schemes for ultra Low-Voltage SRAM circuits.

7. a) With the help of schematic and toning diagrams explain about Armulator.
   b) Give the ARM reference peripheral specifications and explain about them.

8. Write notes on any TWO
   a) ARM MMU Architecture
   b) ARM system control processor
   c) Substrate bias voltage V_{BB} generator.

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